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MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE--ETC(U)
JAN 79 B G GORDON DAAB07-76-C-0041

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TENTH QUARTERLY PROGRESS REPORT

1 OCTOBER 1978 TO 31 DECEMBER 1978

CONTRACT DAAB07 - 76 - C - 0041

# MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE HYBRID MULTIPLIER MODULES

PLACED BY:

NIGHT VISION AND ELECTRO - OPTICAL LABORATORIES

U.S. ARMY ERADCOM, FORT BELVOIR, VA., 22060



CONTRACTOR:

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Data is presented on material and fixtures used in the fabrication of the multiplier modules.
The technique of silk screening the conductive epoxy onto the components is described in the fabrication of the voltage multiplier.

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1 OCTOBER 1978 TO 31 DECEMBER 1978

# MANUFACTURING METHODS AND TECHNIQUES FOR MINIATURE HIGH VOLTAGE HYBRID MULTIPLIER MODULES

CONTRACT NO. DAAB07 - 76 - C - 0041

PREPARED BY: B. GRANT GORDON, P.ENG.

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## ABSTRACT

The progress made during the tenth quarter of work on the Manufacturing and Technology Programme for Miniature High Voltage Multiplier Modules is described in this report.

Data is presented on material and fixtures used in the fabrication of the multiplier modules.

The technique of silk screening the conductive epoxy onto the components is described in the fabrication of the voltage multipliers.

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## PURPOSE

This Contract covers component designs, mounting and interconnection techniques, tooling and test methods and other manufacturing methods and techniques required for production of rectangular and curved miniature high voltage multiplier modules. These units are to be used in low cost power supplies for image intensifier tubes. The full scope and details of the specification are given in Appendix A to the Eighth Quarterly Report.

Major milestones in this program consist of delivery of the following items:

(1) First and second engineering samples and test data.

(2) Production line layout and schedule.

(3) Confirmatory samples and test data.

(4) Production line set-up.

(5) Pilot production run.

(6) Production rate demonstration.

(7) Preparation and publication of a final report.

The general approach is to design and set-up a cost-effective production capability, utilizing already established device technologies and materials, and to demonstrate the production line capability to fabricate at the rate of 125 acceptable units per 40 hour week.

## GLOSSARY OF SPECIAL TERMS

| | |
|---|---|
| Capacitor bank: | - Ceramic wafer with metallizations which perform the function of a number of capacitors connected in parallel (parallel bank) or in series (series capacitor bank). |
| Cure: | - To change the physical properties of a material by chemical reaction or by the action of heat and catalyst. |
| Flash test: | - Test consisting of instantaneous application of voltage at its specified value to the part. |
| Hybrid: | - Technology combining thick-films (capacitor banks) with discrete devices (rectifiers). |
| Multiplier Modules: | - Device consisting of capacitor banks and rectifiers connected and packaged to perform voltage multiplication and rectification. |
| Pad: | - The metallized area on the ceramic bank acting as a plate of a capacitor and used to make an electrical connection to it. |
| Rectifier: | - Semiconductor device with one or more p-n junctions connected in series. |
| Rectifier-substrate Assembly: | - A substrate with rectifiers placed and secured within it. |

Substrate: - Part of a multiplier module consisting of a piece of insulating material machined to accommodate the rectifiers and support the capacitor banks.

## LIST OF SYMBOLS AND ABBREVIATIONS

ic - charging current ($\mu A$)

$C_x$ - measured capacitance (pF)

D.F. - dissipation factor (%)

f - frequency (KHz)

$C_i$ - input capacitance (pF)

$I_L$ - load current (nA)

$v_r$ - ripple voltage (V)

$V_B$ - breakdown voltage (V)

$V_i$ - input voltage (Vp-p)

$V_o$ - output voltage (V d.c.)

$\eta$ - efficiency (%)

$V_F$ - rectifier forward voltage drop (V)

PTRV - peak transient reverse voltage (V)

$I_R$ - rectifier leakage current (nA)

## 1. INTRODUCTION

This report describes briefly the progress in the Manufacturing Methods and Techniques for Miniature High Voltage Hybrid Multiplier Modules Program, made during the latest calendar quarter.

In the First Quarterly Report the design and the manufacturing process for rectangular and curved multiplier modules were described. Prototype rectifier-substrate assemblies were fabricated and then redesigned to simplify the assembly operation. The specification covering the requirements for the multiplier modules forms Appendix A of the Report.

In the Second Quarterly Report results of the electrical evaluation of the first sample batch of rectangular capacitor banks TSK 25-250 and TSK 25-251 were given, the choice of the rectifier was made and electrical test results were presented on non-modular multipliers fabricated with TSK 25-250 and TSK 25-251 capacitor banks and standard HV20PD four-junction rectifiers, to evaluate these components.

In the Third Quarterly Report results of electrical tests on rectangular multiplier modules were presented.

For an input voltage of 1 KV, efficiencies above 96% under no-load conditions and above 95% with 500 nA load currents were achieved for all multipliers assembled with TSK 25-250 and TSK 25-251 and three-chip rectifiers. Low ripple voltages, input capacitances and charging currents were also measured on these multipliers. Results of the mechanical and electrical evaluation of TSK 25-249 curved capacitor banks were also presented in the Third Quarterly Report.

In the Fourth Quarterly Report work on impregnation and coating of the multipliers was discussed as well as some problems associated with the fabrication of the rectifier-substrate assemblies. The fabrication of rectangular and curved multipliers for the First Engineering Sample was discussed.

In the Fifth Quarterly Report were presented the results of electrical performance testing at the room, high (+52$^{\circ}$C) and low (-54$^{\circ}$C) temperatures, as well as effects of thermal shock, and high and low temperature storage.

In the Sixth and Seventh Quarterly Reports were presented the results of testing of rectangular and curved multipliers to the Second Engineering Sample requirements,

steps to improve the frequency performance of the multipliers and optimization of the rectifiers for these devices, as well as results of life testing of multipliers.

In the Eighth Quarterly Report the results of the reliability testing of rectangular and curved multipliers to the Second Engineering Sample requirements were analyzed and further steps to improve the performance of the multipliers and optimize the rectifiers for these devices were discussed.

In the Ninth Quarterly Report the results of further life-testing of rectangular and curved multipliers was discussed. The commencement of the Confirmatory Sample phase was described including improvements in the manufacturing methods.

## 2. FABRICATION AND EVALUATION OF MULTIPLIERS

### 2.1 Substrate Assembly

The first batch of 38 substrate assemblies experienced manufacturing difficulties and were rejected. The 20 rectangular assemblies were correctly assembled manually (as per Engineering Samples) but all exhibited some faults. Each unit had several rectifiers in it (after processing) which did not meet the specifications on forward voltage drop ($V_F$), peak transient reverse voltage (PTRV) and/or leakage current ($I_R$). The failures were characterized by a $V_F$ that was either very resistive or open, a PTRV of less than 1000 volts or an $I_R$ of greater than 100 nA. (Specified values are 2.5 to 4.5V for $V_F$ at 10 mA, 1500 Vpp minimum for PTRV and 7 nA maximum for $I_R$ at 1000V bias.) A failure analysis on these substrates showed two problems: an overlapping of the substrates and a number of voids in the encapsulating epoxy. The overlapping condition exposed the silicon of some rectifiers and caused improper contact, thus, giving high values for $V_F$ . The epoxy voids caused "arc-over" at the PTRV test and allowed a high $I_R$ due to the exposed surface between anode and cathode.

The 18 curved substrates were incorrectly assembled (i.e. all the rectifiers were reversed), as the

result of an operator error. They were examined anyway and exhibited essentially the same problems as the rectangular units: overlapping and epoxy voids.

Then a second batch of 40 substrates was assembled; 20 rectangular and 20 curved types. More control was exercised on this lot and the results were far better although there were several reversed diodes and some overlapping of the substrates. Therefore, we started a batch of 20 voltage multipliers - 10 of each type. Unfortunately all 20 parts failed at the first inspection on $V_F$. All but 1 of the assemblies were "open" although 2 had continuity at the correct value but in the wrong polarity and a third unit had a low value of $V_F$ indicating a short of one or more diodes in the substrate. A failure analysis showed the major problem to be excessive conductive epoxy at the substrate lead slots and since this is cured in advance of the assembly operation, the excess prevented the DC capacitor from making proper contact with the substrates. The curved multipliers had an additional problem in that the substrates were placed in the "sandwich" configuration backwards so that the $V_F$ was reversed from the correct value - another operator error.

These 20 parts were reworked however we only achieved 1 working unit (curved) while 18 of the others were either "open" or "shorted" and 1 unit had a low $V_F$ - indicative of a short of one or more diodes on the substrate assembly.

A failure analysis of these parts showed two problems: epoxy build-up at the slots (as had happened on the original manufacture) and epoxy "smearing" on the contacting surfaces so that "bridges" or "shorts" were created.

Meanwhile another group of 80 substrate assemblies (40 of each type) were then fabricated. We achieved much better results, especially on the last batch of 40 parts for which we had de-aired the encapsulating epoxy prior to use in addition to the normal vacuum - de-airing during the potting of the substrates.

Due to our previous problems with the multiplier manufacture using manual assembly, we investigated several alternatives and decided upon a silk screen technique as our most feasible approach. The basic idea is relatively simple as it is merely the application of a thin layer of the Epo-Tek epoxy (less than .001") onto both the ceramic capacitors and the

rectifier-substrate assembly. This entails that 4 layers of epoxy are deposited on the various surfaces; two of which can use the same screen that the Ceramic group uses for printing the electrode pattern on the capacitor itself and the other two of which require a screen which is the mirror image of the first one. We have proved that the silk screen technique will work insofar as a controlled deposition of epoxy in a specified location is concerned and we now require the second screen to complete our evaluations. The various screens were placed on order with Erie, Pa. and received at the end of December. In addition a fixture was designed to hold the various components in place by use of a vacuum while the epoxy is being silk screened onto its surface. The fixture was built in our model shop and proved on our capacitors and substrates. The silk screen procedure and holding fixture are illustrated in Fig. 7.

Further, the fixture for holding the rectangular substrates during loading and encapsulating of the diodes has been modified slightly to include a base-plate (for better stability) and an improved cavity

outline (to allow easier unloading of the cured substrate assemblies). The fixture is illustrated in Fig. 6.

## 2.2 Production Materials

As sufficient rectifiers had been fabricated with the thin nailhead lead (HVRO4M-13) without problems, I released the remaining 50,000 pieces of the order to Emporium Specialties for this part with a scheduled delivery of early January 1979.

By the end of December we had received 2640 rectifiers (type HSC-3, part number RD0058). These devices are now being stockpiled for later use in the Confirmatory Sample and Pilot Production Run.

The substrate plates (P/N TSK-312-104 and TSK-313-104) have been modified slightly for ease of manufacture (see Fig. 4 and 5) and RFQ's were sent out to several vendors including the manufacturer of the Vespel SP-1 polyimide, Dupont. We should receive their responses in the early part of the new year and, if satisfactory, we will place an order for sufficient parts to cover the Pilot Production Run.

We have received the first batch of capacitors, P/N TSK-25-260 (lot #850066), manufactured by the Erie Trenton Ceramic Production Group. The electrical measurements are given in Table 1 and the mechanical characteristics in Table 2 and Fig. 1, 2 and 3.

In general the capacity is higher and the breakdown voltage lower compared to capacitors supplied by Erie, Pa. The ceramic engineers involved in this project have assured me that the $V_B$ can be increased and we should see higher readings on the next parts supplied to us.

Mechanically, the samples do not meet all the print dimensions in several areas especially the bank thickness, total arc length and electrode pattern screening. Sample B was an example of a mis-screened capacitor and the entire lot had to be sorted for correct registration of the electrode pattern. Therefore the number of acceptable capacitors amounted to 219 pieces. The ceramic engineers have indicated that they will work on improving the dimensions for the next batch of capacitors to be delivered.

An additional test was performed on the capacitors to check the dielectric qualities of the ceramic: 10 capacitors were fabricated into 5 voltage multipliers of a standard (rather than miniature) configuration using a regular Erie diode, HV30P. These parts were tested in Fluorinert dielectric fluid and the results are listed in Table 3. These results show a very good efficiency and breakdown voltage on all multipliers.

## 3. CONCLUSIONS

The material problems are being solved and the appropriate quantities of components to complete the Pilot Production Run are in manufacture or on order from outside vendors with the exception of the substrates which are out on RFQ's at this time.

The technique of silk screening epoxy onto the components as part of the fabrication of the voltage multipliers appears to be a feasible one and will be utilized in further investigation.

## 4. PROGRAMME FOR NEXT QUARTER

4.1 Ascertain the validity and usefulness of the silk screen procedure.

4.2 Initiate manufacture of confirmatory sample voltage multiplier modules.

4.3 Commence testing on confirmatory sample multipliers.

## 5. PUBLICATIONS AND REPORTS

No reports or publications were made on the work associated with this program during the current quarter.

## 6. IDENTIFICATION OF PERSONNEL

Brief descriptions of the background of technical personnel involved were included in the preceding Quarterly Progress Reports.

During the Ninth quarter of the program the following persons worked in their area of responsibility:

| INDIVIDUAL | RESPONSIBILITY | HRS. SPENT |
|---|---|---|
| B.G. Gordon | Programme Manager | 158 |
| D. Platt | Manager, Quality Assurance and Control, High Voltage Products | 1 |
| D. Archard | Senior Test Technician | 4 |
| K. Cram | Draughtsman | 2 |
| V. Glenn | Q.C. Inspector | 12 |
| C. Grills | Senior Engineering Technician | 72.5 |
| B. Heidt | Process Engineering Supervisor | 4 |
| L. Macklin | Draughtsman | 13 |
| P. Maples | Senior Engineering Technician | 48 |
| D. Regan | Senior Engineering Technician | 16 |
| F. Treverton | Senior Test Technician | 3 |
| | Manufacturing Personnel | 141.1 |

| | | |
|---|---|---|
| TOTAL HOURS | - in quarter | 474.6 |
| TOTAL HOURS | - to date | 4854.0 |

ELECTRICAL TEST DATA FOR TSK - 25 - 260
CURVED CAPACITOR BANK SAMPLES
LOT # 850066

| UNIT # | PAD # | $C_X$ @ 0 KV (pF) | D.F. (%) | $C_X$ @ 6 KV (pF) | $V_B$ (KV) |
|---|---|---|---|---|---|
| A | 1 | 99.3 | 1.55 | 69.5 | 10.8 |
| | 2 | 100.8 | 1.36 | 70.6 | 7.7 |
| | 3 | 101.7 | 1.53 | 71.2 | 8.6 |
| | 4 | 100.6 | 1.28 | 70.4 | 7.7 |
| | 5 | 99.1 | 1.61 | 69.4 | 8.9 |
| | 6 | 100.1 | 1.43 | 70.1 | 7.5 |
| B | 1 | 103.4 | 1.50 | 72.4 | 9.0 |
| | 2 | 111.8 | 1.18 | 78.3 | 8.7 |
| | 3 | 110.0 | 1.24 | 77.0 | 9.0 |
| | 4 | 107.9 | 1.31 | 75.5 | 7.9 |
| | 5 | 117.0 | 1.14 | 81.9 | 7.7 |
| | 6 | 109.1 | 1.17 | 76.4 | 7.9 |
| C | 1 | 102.0 | .87 | 71.4 | 9.5 |
| | 2 | 106.3 | .87 | 74.4 | 9.2 |
| | 3 | 113.9 | .81 | 79.7 | 9.0 |
| | 4 | 110.1 | .80 | 77.1 | 8.2 |
| | 5 | 109.3 | .81 | 76.5 | 9.0 |
| | 6 | 103.0 | .79 | 72.1 | 9.0 |
| Average | | 105.9 | 1.18 | 74.1 | 8.6 |

TABLE 1

MECHANICAL INSPECTION DATA FOR TSK-25-260 CAPACITOR BANKS
LOT # 850066

| UNIT # A | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAD # | | 1 | 2 | 3 | 4 | 5 | 6 |
| A | .2517 | | | | | | |
| B | | .0393 | .0403 | .0392 | .0415 | .0427 | .0441 |
| C | | .0433 | .0422 | .0412 | .0424 | .0384 | .0401 |
| D | | .0504 | .0496 | .0472 | .0481 | .0506 | .0472 |
| E | | .0463 | .0502 | .0464 | .0455 | .0473 | .0463 |
| F | | .0223 | .0237 | .0223 | .0227 | .0233 | .0233 |
| G | .0476 | | | | | | |
| H | .0206 | | | | | | |
| J | .0887 | | | | | | |

| UNIT # B | | | | | | | |
|---|---|---|---|---|---|---|---|
| PAD # | | 1 | 2 | 3 | 4 | 5 | 6 |
| A | .2465 | | | | | | |
| B | | .0730 | .0574 | .0443 | .0307 | .0174 | .0085 |
| C | | .0233 | .0360 | .0503 | .0644 | .0778 | .0878 |
| D | | .0458 | .0453 | .0435 | .0439 | .0427 | .0436 |
| E | | .0446 | .0443 | .0440 | .0435 | .0443 | .0441 |
| F | | .0202 | .0201 | .0205 | .0199 | .0193 | .0187 |
| G | .0423 | | | | | | |
| H | .0220 | | | | | | |
| J | .1085 | | | | | | |

Notes: (i) All dimensions in inches.
(ii) See Fig. 3 for dimensioning.

TABLE 2

TSK-25-260 CAPACITOR

ELECTRODE PATTERN DIMENSIONS

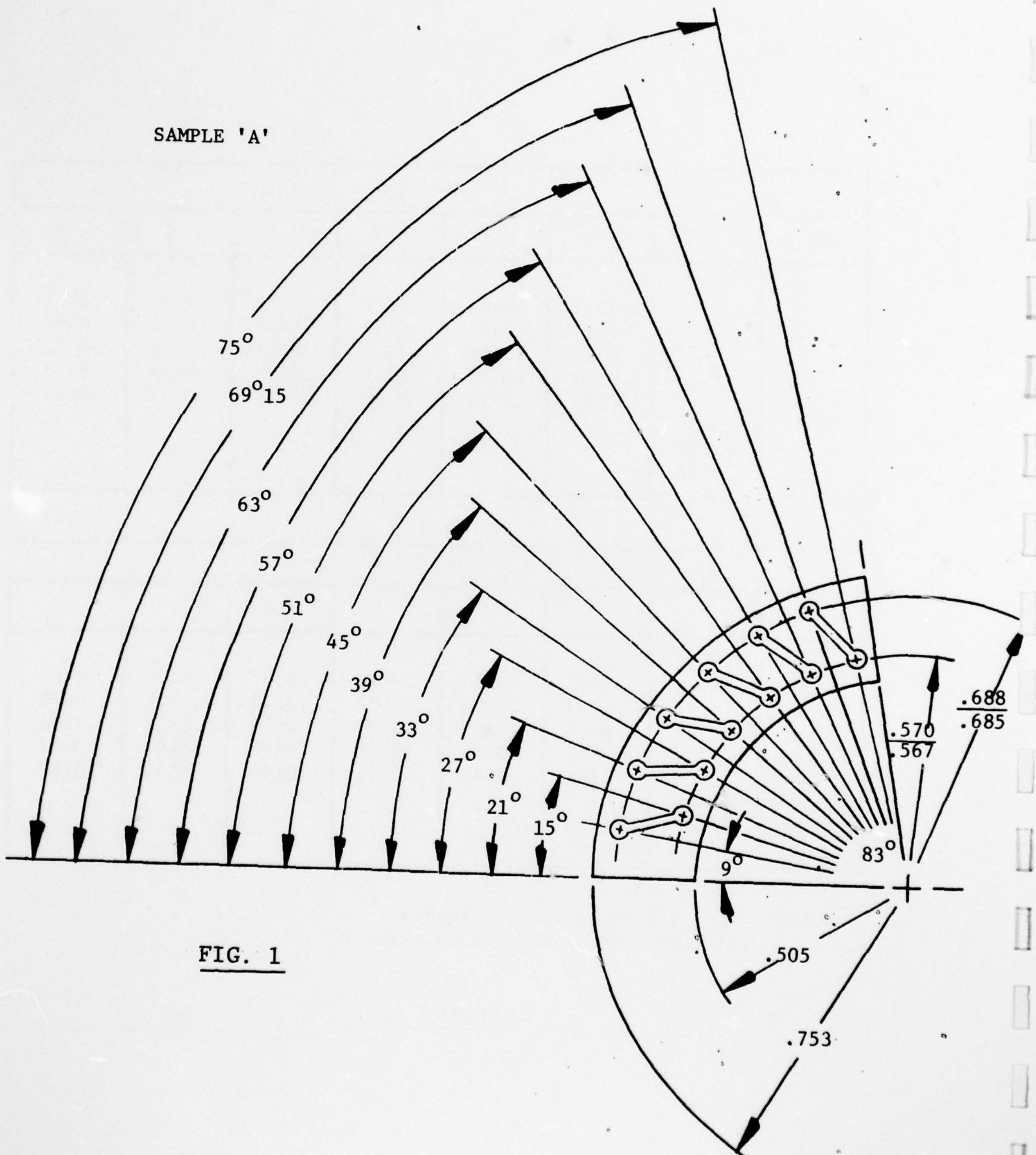



FIG. 1

TSK-25-260 CAPACITOR

ELECTRODE PATTERN DIMENSIONS

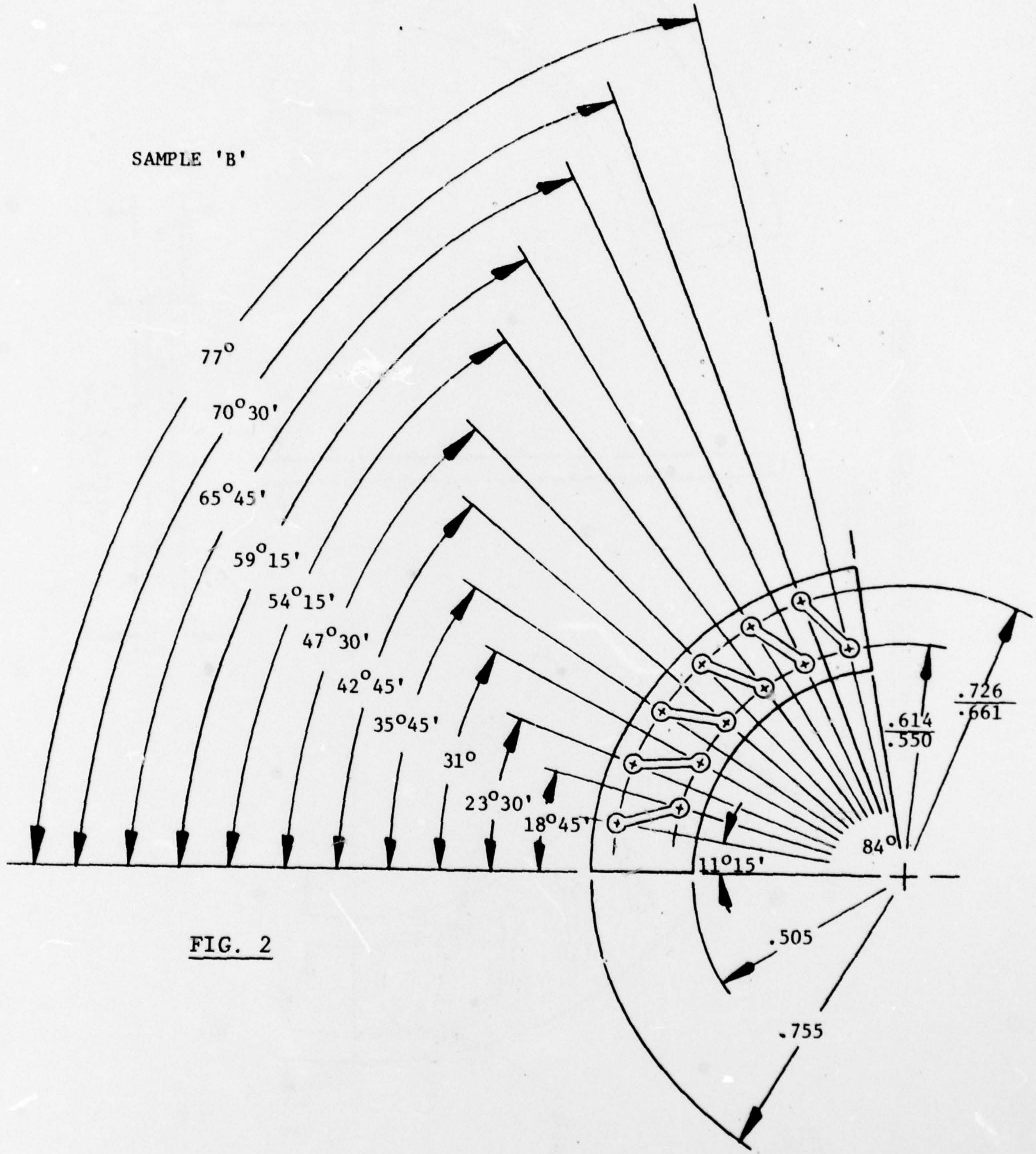
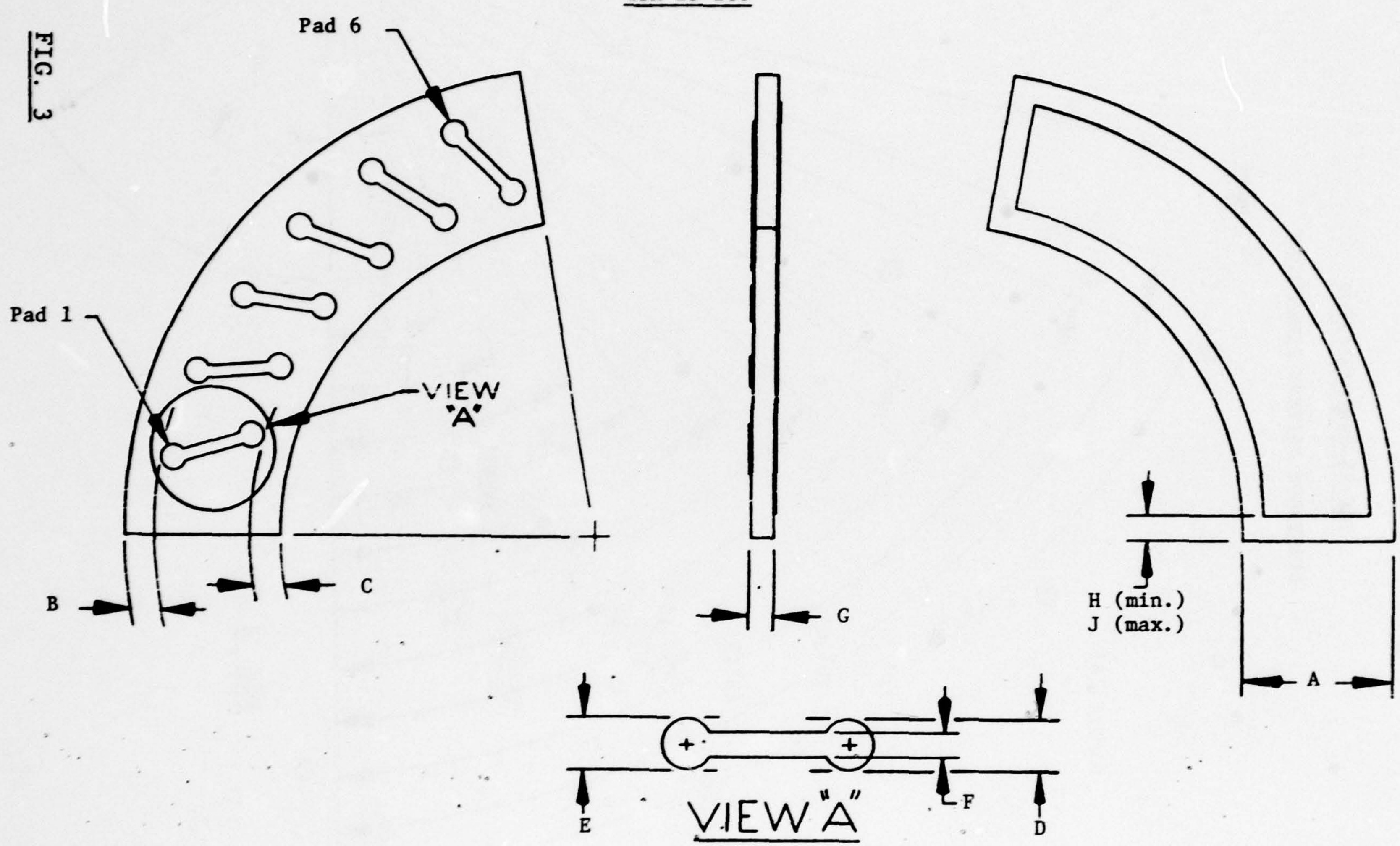



FIG. 2

FIG. 3

DIMENSIONING OF CURVED BANK CAPACITORS

TSK-25-260

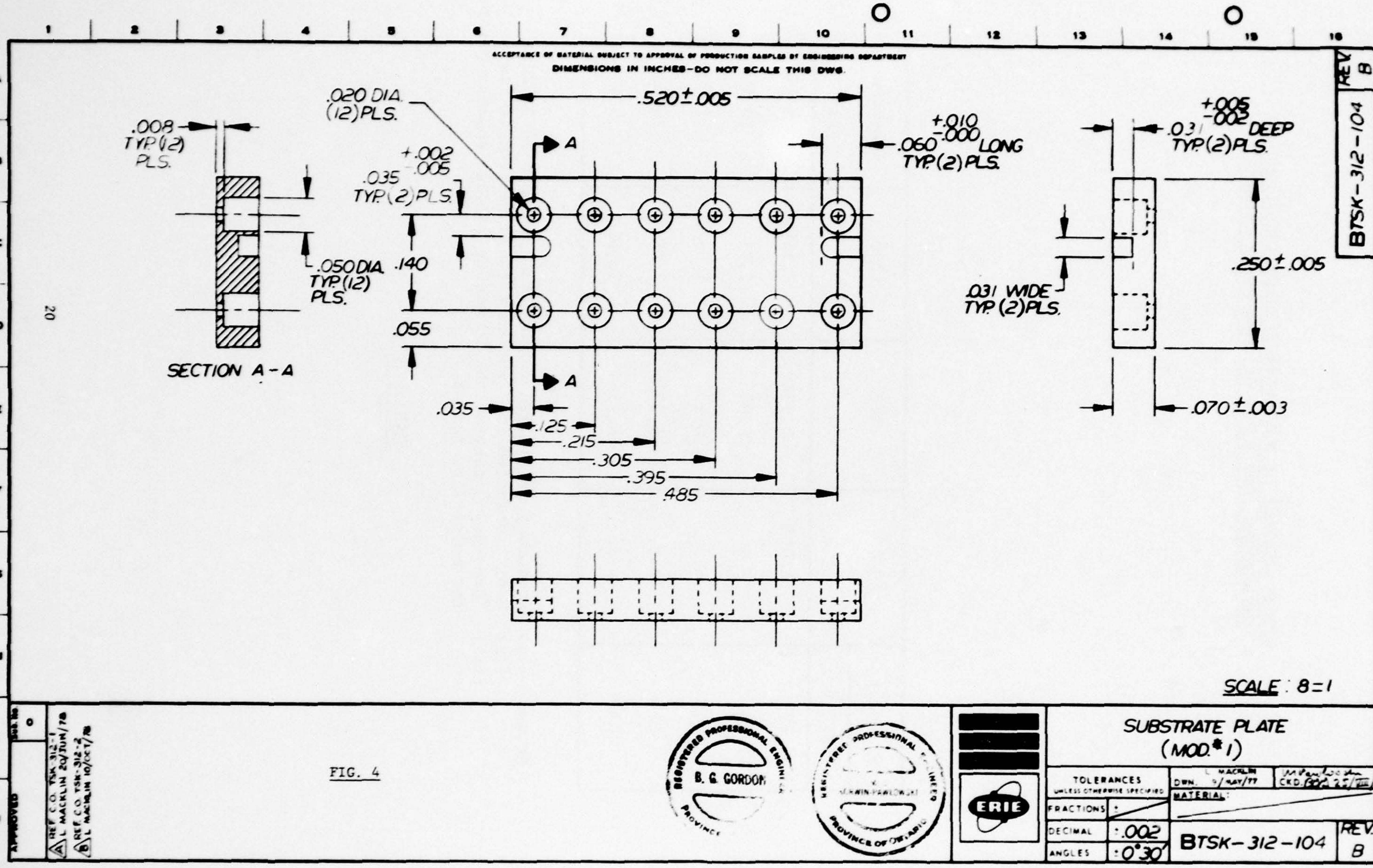


OUTPUT VOLTAGE OF MULTIPLIERS USING TSK-25-260 CAPACITORS (LOT # 850066) AND HV30P DIODES

| $V_i$ ($V_{pp}$) / UNIT # | 1000 | 1150 | 1300 | Breakdown (iii) |
|---|---|---|---|---|
| 29 | 6.0KV | 6.95KV | 7.95KV | 9.4KV |
| 30 | 6.0 | 6.95 | 7.95 | 10.3 |
| 31 | 6.0 | 6.95 | 7.95 | 9.3 |
| 32 | 6.0 | 6.95 | 7.95 | 8.0 |
| 33 | 6.0 | 6.95 | 7.95 | 9.4 |

Notes:
(i) Frequency of applied voltage in all tests is 35 KHz.
(ii) Tests conducted in Fluorinert FC-43 dielectric fluid.
(iii) "Breakdown" denotes the DC output voltage reached before the multiplier failed.

TABLE 3



ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
DIMENSIONS IN INCHES—DO NOT SCALE THIS DWG.
.020 DIA. (12) PLS.
.520 ± .005
.008 TYP. (12) PLS.
+.002 −.005 .035 TYP. (2) PLS.
.050 DIA. TYP. (12) PLS.
.140
.055
SECTION A-A
A
A
+.010 −.000 .060 LONG TYP. (2) PLS.
+.005 −.002 .031 DEEP TYP. (2) PLS.
.031 WIDE TYP. (2) PLS.
.250 ± .005
.070 ± .003
.035
.125
.215
.305
.395
.485
SCALE: 8=1
REF. C.O. TSK-312-1 L. MACKLIN 20/JUN/78
REF. C.O. TSK-312-2 L. MACKLIN 10/OCT/78
APPROVED
B. G. GORDON
ERIE
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ±
DECIMAL ±.002
ANGLES ±0°30'
SUBSTRATE PLATE (MOD. # 1)
DWN. L. MACKLIN 9/MAY/77
MATERIAL:
BTSK-312-104
REV. B


FIG. 4

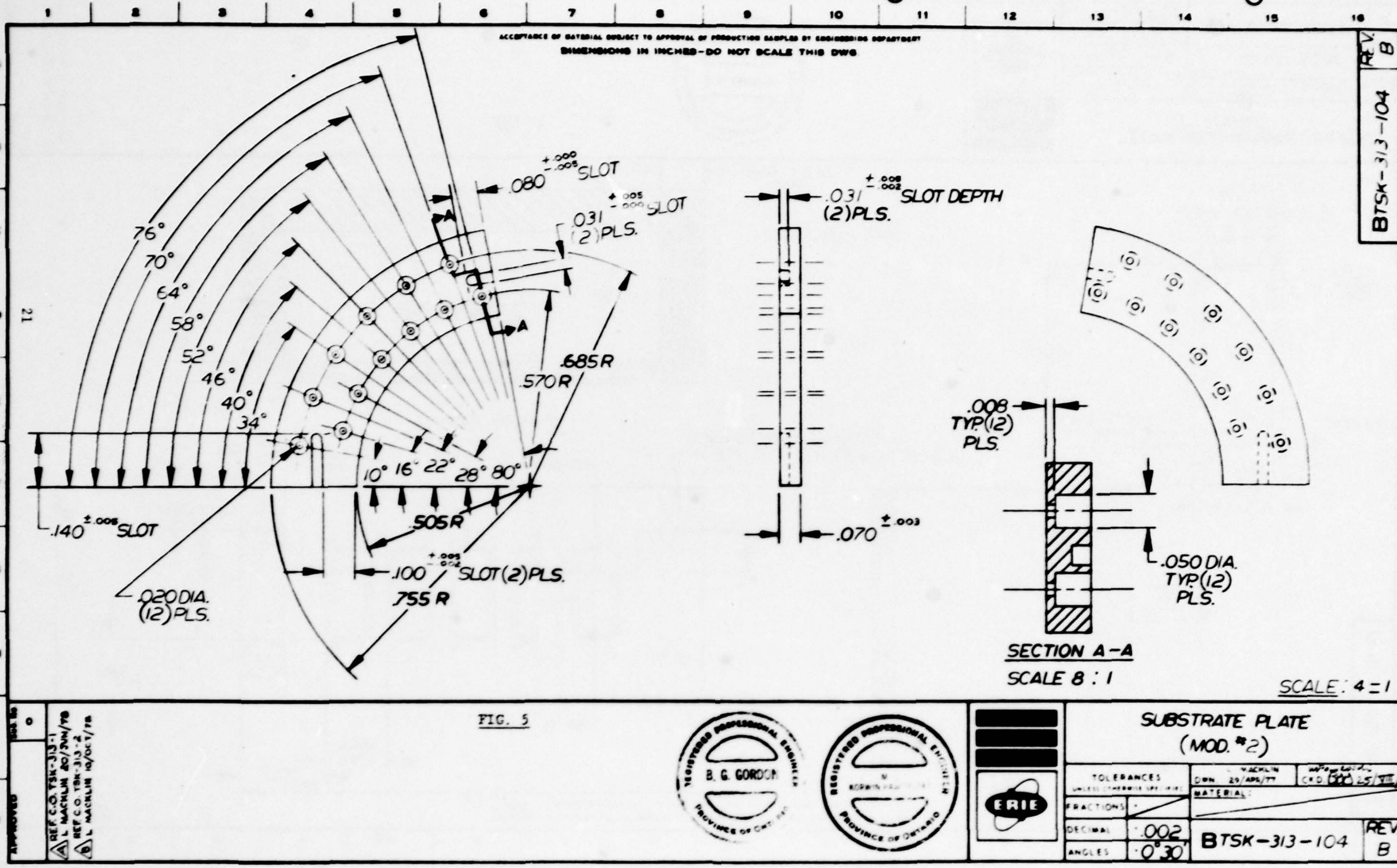
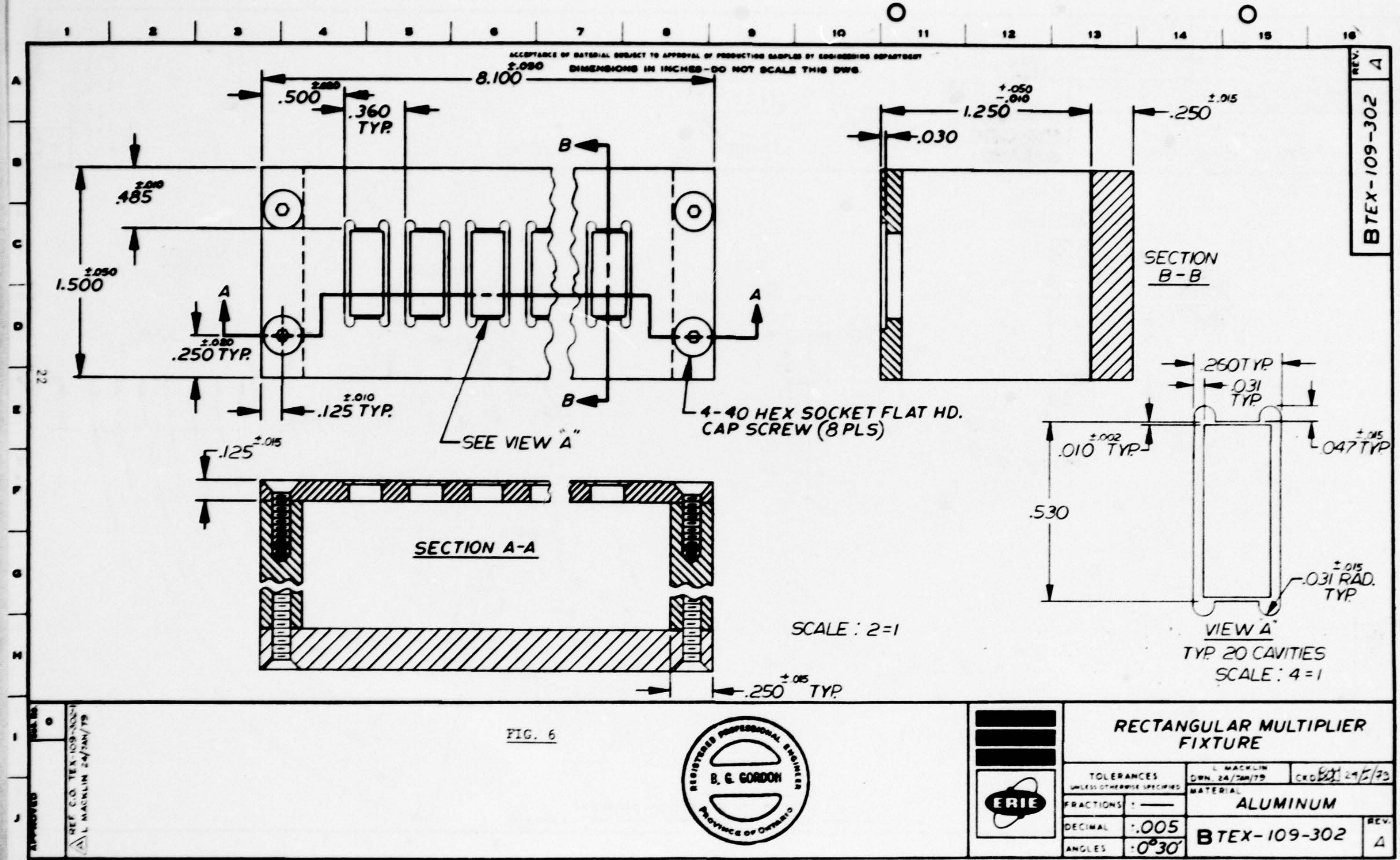

ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
DIMENSIONS IN INCHES-DO NOT SCALE THIS DWG
76°
70°
64°
58°
52°
46°
40°
34°
10° 16° 22° 28° 80°
.080 +.000 -.005 SLOT
.031 +.005 -.000 SLOT (2) PLS.
.685 R
.570 R
.505 R
.755 R
.140 ±.005 SLOT
.020 DIA. (12) PLS.
.100 +.005 -.002 SLOT (2) PLS.
.031 +.008 -.002 SLOT DEPTH (2) PLS.
.070 ±.003
.008 TYP. (12) PLS.
.050 DIA. TYP. (12) PLS.
SECTION A-A
SCALE 8 : 1
SCALE: 4=1
SUBSTRATE PLATE
(MOD. #2)
TOLERANCES
FRACTIONS
DECIMAL .002
ANGLES 0°30'
DWN 29/APR/77
MATERIAL:
BTSK-313-104
REV B
B. G. GORDON
PROVINCE OF ONTARIO
ERIE
REF C.O. TSK-313-1 L. MACKLIN 20/JUN/78
REF C.O. TSK-313-2 L. MACKLIN 10/OCT/78
APPROVED

FIG. 5


ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT
DIMENSIONS IN INCHES-DO NOT SCALE THIS DWG.
8.100 ±.030
.500 ±.010
.360 TYP.
.485 ±.010
1.500 ±.050
.250 TYP. ±.030
.125 TYP. ±.010
SEE VIEW "A"
4-40 HEX SOCKET FLAT HD. CAP SCREW (8 PLS)
.125 ±.015
SECTION A-A
SCALE : 2=1
.250 ±.015 TYP.
1.250 +.050 −.010
.030
.250 ±.015
SECTION B-B
.260 TYP.
.031 TYP.
.010 ±.002 TYP.
.047 ±.015 TYP.
.530
.031 ±.015 RAD. TYP.
VIEW "A"
TYP. 20 CAVITIES
SCALE : 4=1
REF. C.O. TEX-109-302-1
L. MACKLIN 24/JAN/79
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PROVINCE OF ONTARIO
ERIE
RECTANGULAR MULTIPLIER FIXTURE
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± —
DECIMAL ±.005
ANGLES ±0°30'
DWN. L. MACKLIN 24/JAN/79
MATERIAL ALUMINUM
B TEX-109-302
REV. A

FIG. 6

ACCEPTANCE OF MATERIAL SUBJECT TO APPROVAL OF PRODUCTION SAMPLES BY ENGINEERING DEPARTMENT

DIMENSIONS IN INCHES - DO NOT SCALE THIS DWG

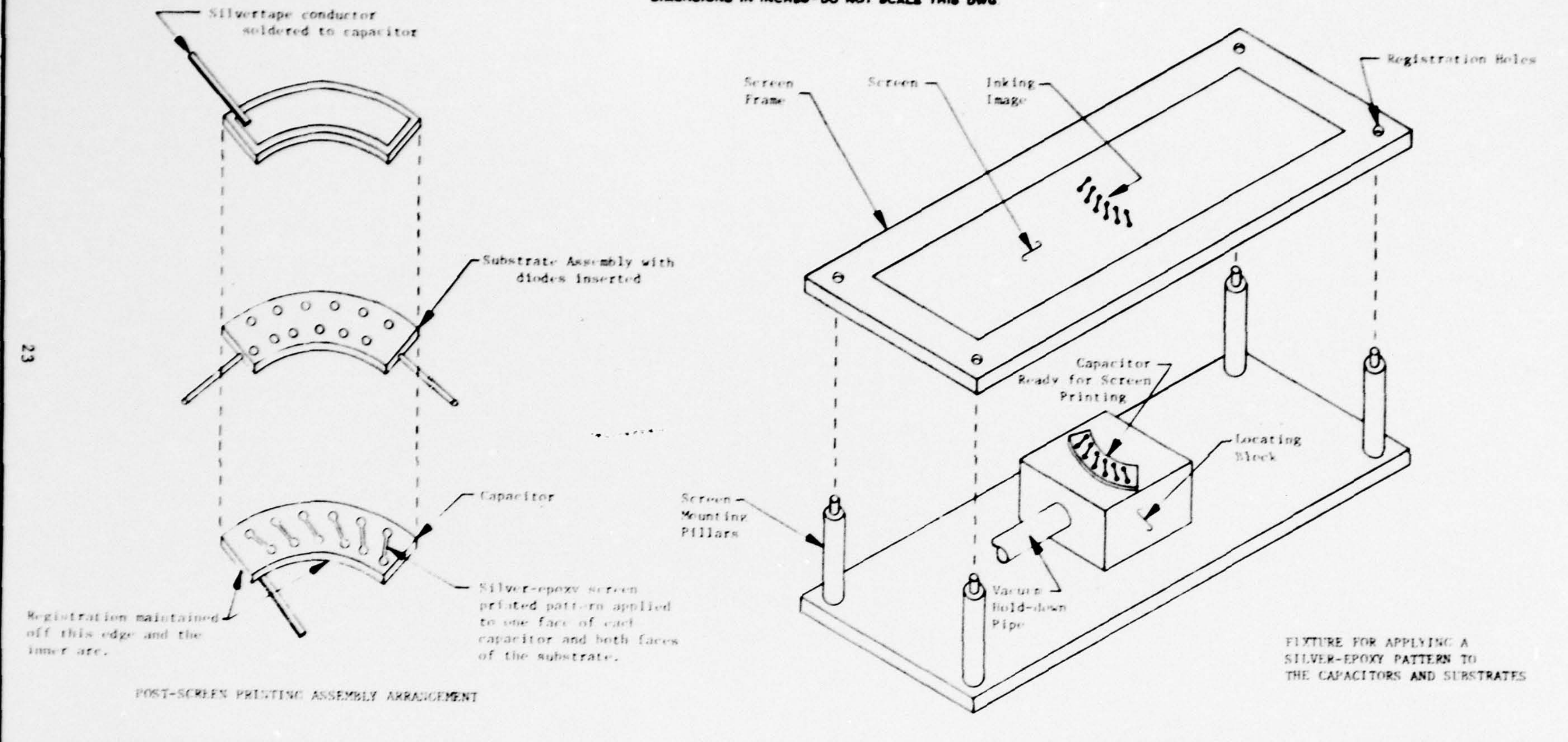


FIG. 7

EPOXY SILK SCREEN

(Curved Bank Multiplier)

| TOLERANCES UNLESS OTHERWISE SPECIFIED | DWN. L.Macklin 23/Jan/79 | CKD |
|---|---|---|
| FRACTIONS | MATERIAL | |
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